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Single- and two-phase heat exchangers for power electronic components

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Abstract — Experiments were performed to assess the feasibility of single-phase and two-phase micro heat sinks applied to the cooling of power components. After a brief recall of the principal characteristics of a power component (IGBT, Insulated Gate Bipolar Transistor), experimental measurements are described for multichip modules cooled by single-phase or two-phase heat sinks machined in a piece of copper. The former is composed of rectangular microchannels, the second is composed of circular minichannels. Both offer very high cooling capabilities. Then, a comparison of performance is presented. © 2000 Éditions scientifiques et médicales Elsevier SAS

single-phase / two-phase / microchannel / power / multichip module

Nomenclature

a	distance between two channels	m
b	channel diameter	m
Cp	specific heat	$J{\cdot}kg^{-1}{\cdot}K^{-1}$
d	distance between the fluid and the chip	m
D	depth of a channel	m
D_h	hydraulic diameter	m
e	width of a fin	m
G	geometrical parameter	
h	heat transfer coefficient	$W{\cdot}m^{-2}{\cdot}K^{-1}$
h_{lv}	latent heat of vaporisation	$J{\cdot}kg^{-1}$
k	thermal conductivity	$W{\cdot}m^{-1}{\cdot}K^{-1}$
L	heat sink length	m
lc	width of a channel	m
m	mass flow rate	$kg{\cdot}s^{-1}$
n	number of channels	
P	power	W
R_{th}	thermal resistance	$K{\cdot}W^{-1}$
s	heat spread effect	
t	device thickness	m
T	temperature	K
W	heat sink width	m
x	quality	

Greek symbol

β	fin efficiency

Subscripts

a	ambient
cap	capacitive
con	convective
i	inlet
j	junction
l	liquid
max	maximum value
o	outlet
sat	saturated
tot	total
w	wall
1D	one-dimensional
3D	three-dimensional

1. INTRODUCTION

Much progress has been made over the past few years in the manufacture of power electronic components, lead-

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ing to an increasing development of IGBTs (Insulated Gate Bipolar Transistors). These components can be easily associated in parallel to reach high current rates. Thus, hybrid modules are composed of elementary chips brazed on the same substrate. For instance, 1 600 V–1 200 A modules with 16 chips can be found.

However, for a given current rating, the number of chips which must be associated in parallel depends on thermal criteria. By improving the cooling of the components, the number of chips decreases, and the compactness of the module can be increased. In these conditions, power electronic components can dissipate heat flux densities up to 400 $W \cdot cm^{-2}$, but their temperature must not overrun 150 °C.

First studied by Tuckerman and Pease [1], water cooled microchannel heat sinks can provide high cooling capabilities, but at the expense of large pressure drops. Bower and Mudawar [2] showed that two-phase micro heat exchangers can also cool components with a high efficiency. Previous works, devoted to the cooling of an IGBT (1 600 V–50 A) by single-phase [3] and two-phase micro heat exchangers [4] integrated under the chip, were extended to a device with four and eight power components.

The aim is to know the electrical and thermal behaviors of hybrid power modules with several chips on the same substrate. After a brief recall on the properties and the use of IGBTs, both heat sinks are presented. Then, their performances are compared.

2. IGBT

IGBT (Insulated Gate Bipolar Transistor) has become the switching device of choice in whole range of power electronic converters. They present low on-state voltage drop and high switching speed. They are capable of operating at frequencies up to 20 kHz. The evolution of the IGBT is turned towards high power applications. IGBT is now available in higher voltage and current ratings. It can control direct voltage up to 3.3 kV. Since it carries large current, the electrical and thermal stresses on the IGBT module increases. For this study, Siemens 50 A–1 600 V IGBT chips (14×14 mm^2) were used.

3. SINGLE-PHASE HEAT EXCHANGER

3.1. Prototype

The prototype is composed of four elementary modules (see *figure 1*). Each elementary module is composed of two IGBT chips directly brazed onto a piece of copper in which microchannels were machined.

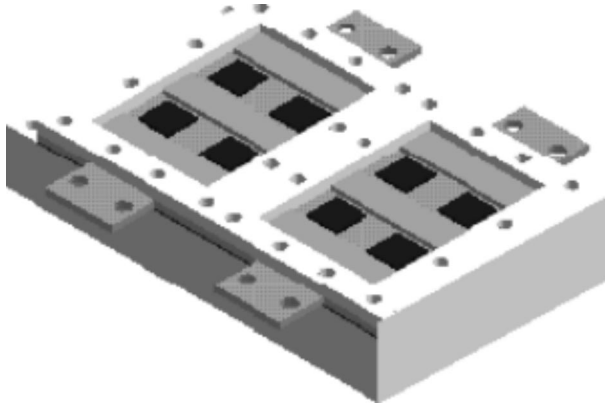

Figure 1. Module with eight IGBT chips.

TABLE I
Sizes of the prototype.

d (mm)	1
D (mm)	2
lc (mm)	0.2
e (mm)	0.2
L (mm)	18
W (mm)	51
n	127

The dimensions of an elementary module are given in *table I*. The geometrical parameters are defined in *figure 2*. The coolant fluid is water with 40 % of glycol to ensure the working of the prototype at low temperature.

3.2. Simulated thermal resistance

The performance of a heat sink is generally measured by its thermal resistance, defined as

$$R_{\text{thtot}} = \frac{T_{\text{w,o}} - (T_{\text{l,i}} + T_{\text{l,o}})/2}{P} \quad (1)$$

where $T_{\text{w,o}}$ is the outlet wall temperature, $T_{\text{l,i}}$ and $T_{\text{l,o}}$ are the inlet and outlet liquid temperatures.

The resistance can be split into two components:

$$R_{\text{thtot}} = R_{\text{thcap}} + R_{\text{thcon}} \quad (2)$$

R_{thcap} is due to the heating of the fluid as it absorbs energy passing through the heat exchanger: R_{thcon} is due to heat conduction in the fins and convection from the fins to the fluid.

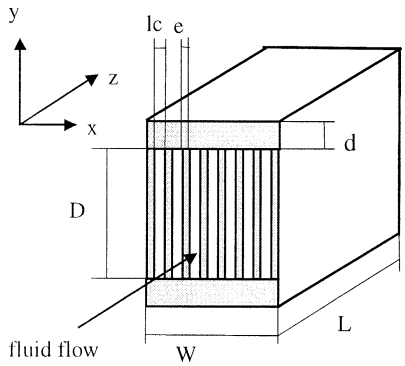

Figure 2. Microchannel setup. Geometrical parameters.

Generally, a one-dimensional analysis is used to obtain thermal resistances:

$$R_{\text{thcap}} = \frac{1}{m\,Cp} \tag{3}$$

$$R_{\text{thcon}} = \frac{1}{hnL(2\beta D + lc)} + \frac{d}{k_{\text{w}} WL} \tag{4}$$

where

$$\beta = \frac{\tanh(\sqrt{2h/ek_{\text{w}}}\,D)}{\sqrt{2h/ek_{\text{w}}}\,D} \tag{5}$$

The heat transfer coefficient h can be obtained from correlations according to the nature of the flow and the dimensions of the channels. For the flow rates considered in the study, the fluid flow was laminar. The corresponding correlations [5] were used to calculate the heat transfer coefficient h.

In the case of rectangular channels, for a laminar fluid flow, without thermal and hydraulic entrance effect, if three of the channel walls are uniformly heated and if the fourth is adiabatic, the heat transfer coefficient is given by

$$h = \frac{k_{\text{l}}}{D_{\text{h}}}\left(-14.859 + 65.623G - 71.907G^2 + 29.384G^3\right) \tag{6}$$

with the hydraulic diameter

$$D_{\text{h}} = \frac{2D\,lc}{D + lc} \tag{7}$$

and a parameter G defined as [6]

$$G = \frac{(D/lc)^2 + 1}{(D/lc + 1)^2} \tag{8}$$

From this analytic model, optimisation of the channel sizes can be performed. Generally, the channel sizes are calculated for a given pressure drop or a given pumping power to minimise the total thermal resistance of the heat sink. Genetic algorithms can be used for optimization [5].

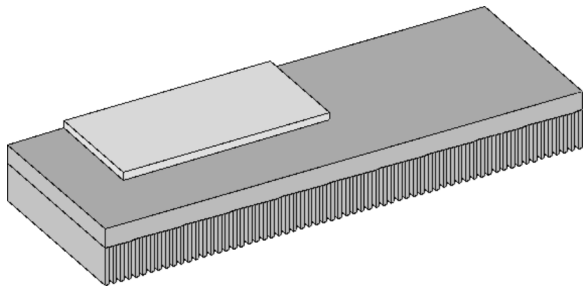

Figure 3. Simulated module.

However, in a multichip module, the microchannels extend beyond the perimeter of heat sources, and heat spreads in three directions. Thus, the one-dimensional approach described above leads to an overestimation of thermal resistance.

Thermal resistance of the chips was calculated with a 3D finite element simulation tool called FLUX 3D to take into account thermal spreading. FLUX 3D is a software developed in our laboratory. It takes into account thermal conduction in the different layers of the device and convection with the ambient, and calculate the temperature in each point of the module. Convection is characterised by the heat transfer coefficient h. We simulated a quarter of an elementary module (see *figure 3*), with half of a chip (thickness 300 μm, thermal conductivity 100 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$), a brazed layer under the chip (thickness 50 μm, thermal conductivity 30 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$), and a copper heat sink with the microchannels. A heat transfer coefficient h is applied on three walls of the channels to model the convection between the fluid and the walls.

The estimated thermal resistance is calculated as

$$R_{\text{th3D}} = \frac{T_{\text{j}} - T_{\text{a}}}{P} \tag{9}$$

where P is the power dissipated in the chip, T_{j} is the mean temperature in the volume of the chip and T_{a} is the ambient temperature.

The effect of heat spread can be calculated by comparing the 1D approach and the 3D approach. A parameter s, which represents heat spread effect, is defined as

$$s = \frac{R_{\text{th1D}} - R_{\text{th3D}}}{R_{\text{th1D}}} \tag{10}$$

The parameter s is plotted in *figure 4* as a function of heat transfer coefficient. For microchannel cooling, the heat transfer coefficient is in the region

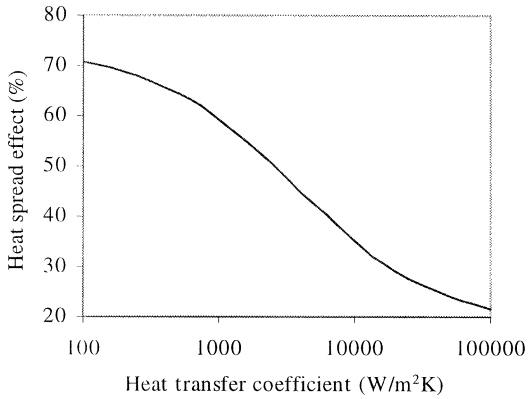

Figure 4. Heat spread effect.

of 10^4 W·m^{-2}·K^{-1}, and the heat spread effect is higher than 35 %. This result shows that a 3D approach is required to predict thermal resistance with a good accuracy.

3.3. Results

The measurement loop is presented in *figure 5*. The flow rate is controlled by means of a valve and is measured with a flowmeter. Inlet and outlet fluid temperatures are obtained with thermocouples. The pressure drop in the exchanger is given by a manometer.

As the power chips are associated in parallel, it is difficult to estimate the junction temperature from the calibration of the electrical parameters of the component [4]. Then, the temperature measurement was performed by means of an infrared camera and only the chip surface temperatures were obtained.

The chips were recover with a black paint to limit the radiative thermal perturbations and to calibrate temperature measurements. The thermal resistance value of a chip is calculated from measurements according to

$$R_{\text{th,chip}} = \frac{T_{\text{max,chip}} - T_{\text{l,i}}}{P} \qquad (11)$$

where $T_{\text{max,chip}}$ is the maximum temperature detected on the chip surface and P is the power dissipated in the chip.

The thermal resistances were measured for different flow rates and for dissipated power up to 300 W per chip. The thermal resistance as function of fluid flow is shown in *figure 6*. Each point is the average of the eight chip thermal resistances for several values of the dissipated power. The thermal resistance was between 0.09 and 0.11 K·W^{-1} with no significant variation in the power range from 50 to 300 W per chip. In other words, the module could dissipate up to 370 W per square centimetre of silicon for a temperature rise between inlet fluid and component of 40 °C. The dissipated power could be increased without overrunning the maximum temperature given by manufacturers on the chip.

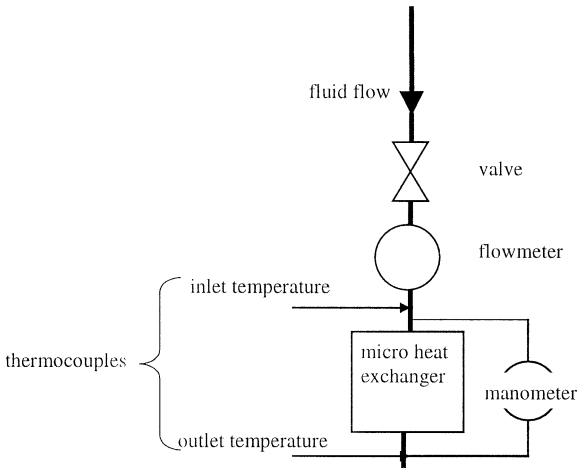

Figure 5. Measurement loop.

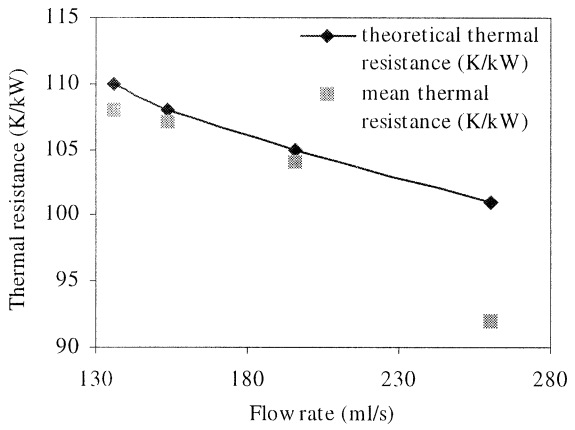

Figure 6. Theoretical and experimental thermal resistances.

The difference between measurements and theoretical values is lower than 10 %, experimental uncertainties are about 10 %.

The pressure drop between the outlet fluid and the inlet fluid as function of flow rate is shown in *figure 7*. It is mainly due to the piping and feed. The pressure drop through the microchannels is almost negligible.

The increase of flow results in an increase of pressure drop with only a slight decrease of thermal resistance.

Another key point is the current sharing between the chips. The eight chips are associated in parallel. We

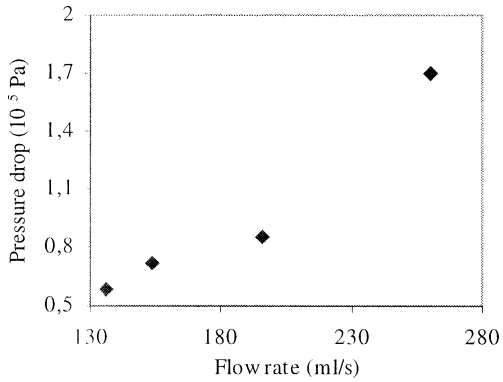

Figure 7. Experimental pressure drop.

notice a difference between the currents of the different elementary modules of about 20 %. This imbalance of the currents can be due to differences between chip intrinsic electrical characteristics or to the brazed layer. We also notice a warm point phenomenon, due to a defective wire bonding. Consequently, there are differences between the thermal resistances of the chips, which lowers the performance of the whole module.

4. TWO-PHASE HEAT EXCHANGER

4.1. Prototype

Four IGBT chips were brazed on a piece of copper in which circular smoothed channels, five per chip, were machined (see *figure 8*). The channel diameter is 2 mm to ensure a high boiling heat transfer coefficient, a high critical heat flux, and a low pressure drop. The criteria given in relation (12) by Bower and Mudawar [2] were applied to ensure a good repartition of heat flux all over the periphery of the channels:

$$a \geq 0.2b \quad \text{and} \quad t \geq 1.1b \tag{12}$$

where a is the distance between two channels, t is the device thickness and b the channel diameter. Simulation in 2D gave results in good accordance with this simplified approach (deviation less than 1 %). As the device had to control current up to 400 A, the source connectors composed of "copper–ceramic–copper" substrates had also to be cooled forcefully: they were brazed above the fluid inlet collectors. The prototype was cooled with water at atmospheric pressure. It was placed horizontally and inserted in an open loop. A condenser was added to the loop described in *figure 5*.

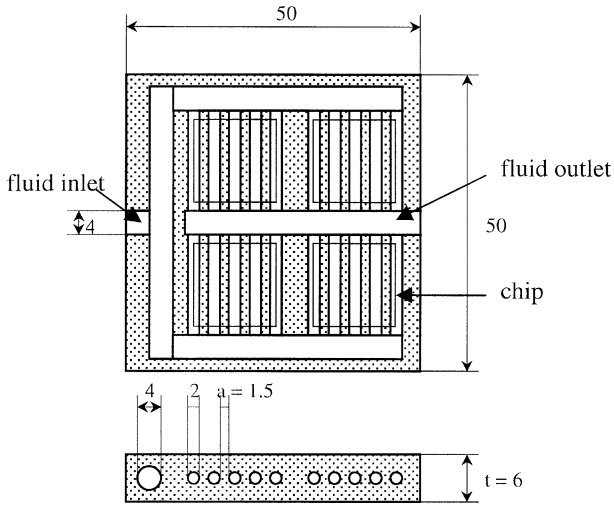

Figure 8. Two-phase setup description (dimensions in mm).

TABLE II
Test conditions for the two-phase device.

Volumetric flow rate (ml·min^{-1})	Maximum dissipated power (W)	Outlet vapor quality
80	850	0.225
170	1250	0.156
216	2950	0.35

The outlet quality of the vapour (13) obtained via the thermal balance is limited to 0.3 to prevent flow instability and local dry-out. This condition set a minimum flow rate. Moreover, the flow rate must be as low as possible to limit the pressure drop.

$$x_{\text{out}} = \frac{P}{m h_{\text{lv}}} - \frac{Cp_{\text{l}}(T_{\text{sat}} - T_{\text{l,i}})}{h_{\text{lv}}} \tag{13}$$

where T_{sat} and $T_{\text{l,i}}$ are respectively the boiling and inlet water temperature, h_{lv} the latent heat of vaporisation, m the mass water flow rate, and P the dissipated power.

4.2. Results

The temperature measurement was performed by means of an infrared camera and only the chip surface temperatures were obtained. Test conditions are listed in *table II*.

The maximum temperature of each chip is plotted in *figure 9* for different flow rates and a dissipated power of about 800 W. It can be seen that the flow rate does not

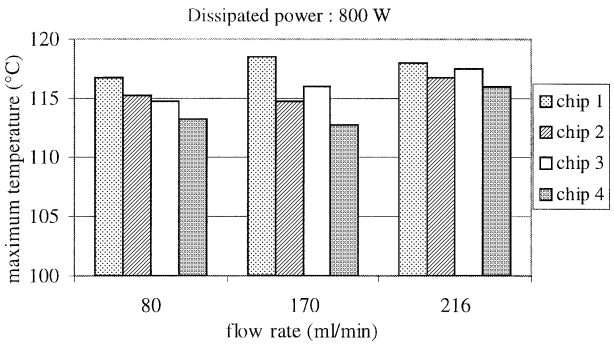

Figure 9. Maximum chip temperature.

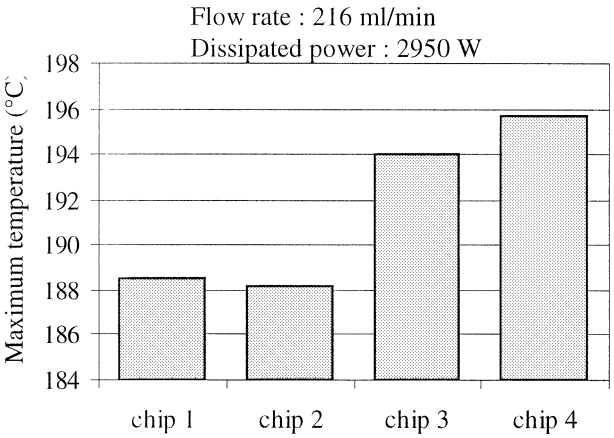

Figure 10. Maximum chip temperature.

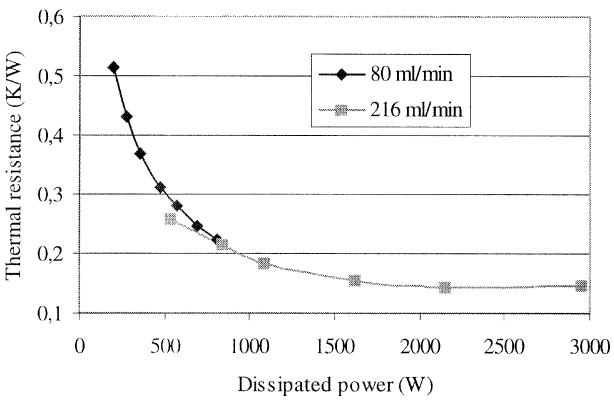

Figure 11. Mean thermal resistance for two flow rates.

influence the chip temperatures, showing that the major part of the heat transfer is due to nucleation.

The maximum temperature of the chips is plotted in *figure 10* for the maximum dissipated power (2 950 W). In these conditions, the chip temperatures overrun the limit temperature defined by manufacturers.

The experimental mean thermal resistance of the chips is plotted in *figure 11* as a function of the dissipated power for two flow rates. The heat transfer coefficient varies with the heat flux density as $\varphi^{0.67}$. Thus, the thermal resistance decreases with the dissipated power. The result is a slight variation of the chip temperatures with the dissipated power. The two-phase device can undergo variable heat load without significant temperature variations and its reliability is increased. At high power densities, temperature rise of the components is lower compared to single phase cooling.

5. CONCLUSION

As components dissipate more and more power with restrictive size constraints, integration of an exchanger directly under the chips is a promising solution. The present study shows that low thermal resistances can be obtained with single-phase and two-phase heat sinks. In both cases, the junction temperature elevation is limited and the switched current can be increased.

In our experimental conditions, with a single phase heat exchanger, the module can dissipate up to 370 W·cm^{-2} for a temperature rise of 40 °C. With a two-phase heat exchanger, about 240 W·cm^{-2} can be dissipated for the same temperature rise.

The results presented in this study for single-phase and two-phase heat exchangers cannot be directly compared. In fact, the surfaces of both prototypes are not the same. As the single phase heat sink is less compact, the spread of heat flux in copper is more important. Thus, the conductive thermal resistance is lower, which lowers the total thermal resistance.

However, the general properties of both heat sinks can be compared. The main advantages of two-phase heat exchangers are:

- to limit the junction temperature excursion according to the power dissipated in the component,
- to require less pumping energy because the flow rates and the pressure drop are lower,
- to be more easily manufactured because the channels are circular and the dimensions are larger (mm).

Nevertheless, the use of two-phase heat exchangers involves more working constraints such as flow instabilities, possibility of local dry-out. Moreover, the putting into practice is more difficult because the fluid must be condensed after heat exchange.

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